

Figure 1: Access/Core Network Diagram

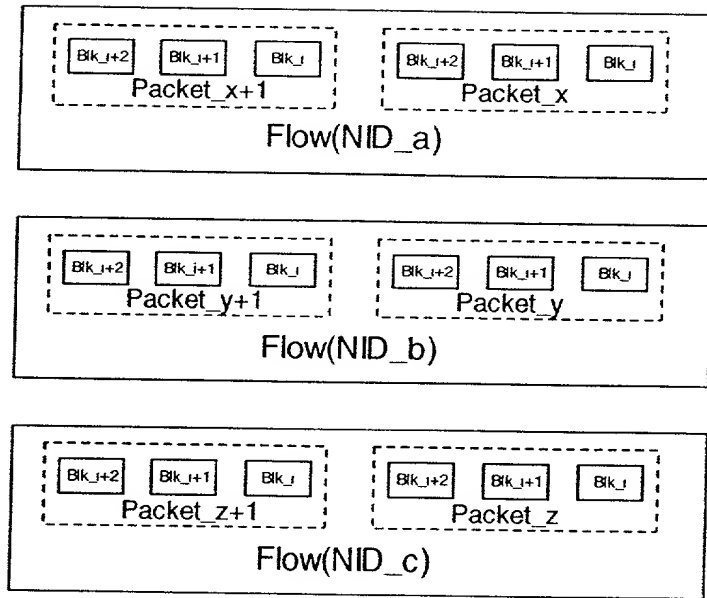


FIG. 2

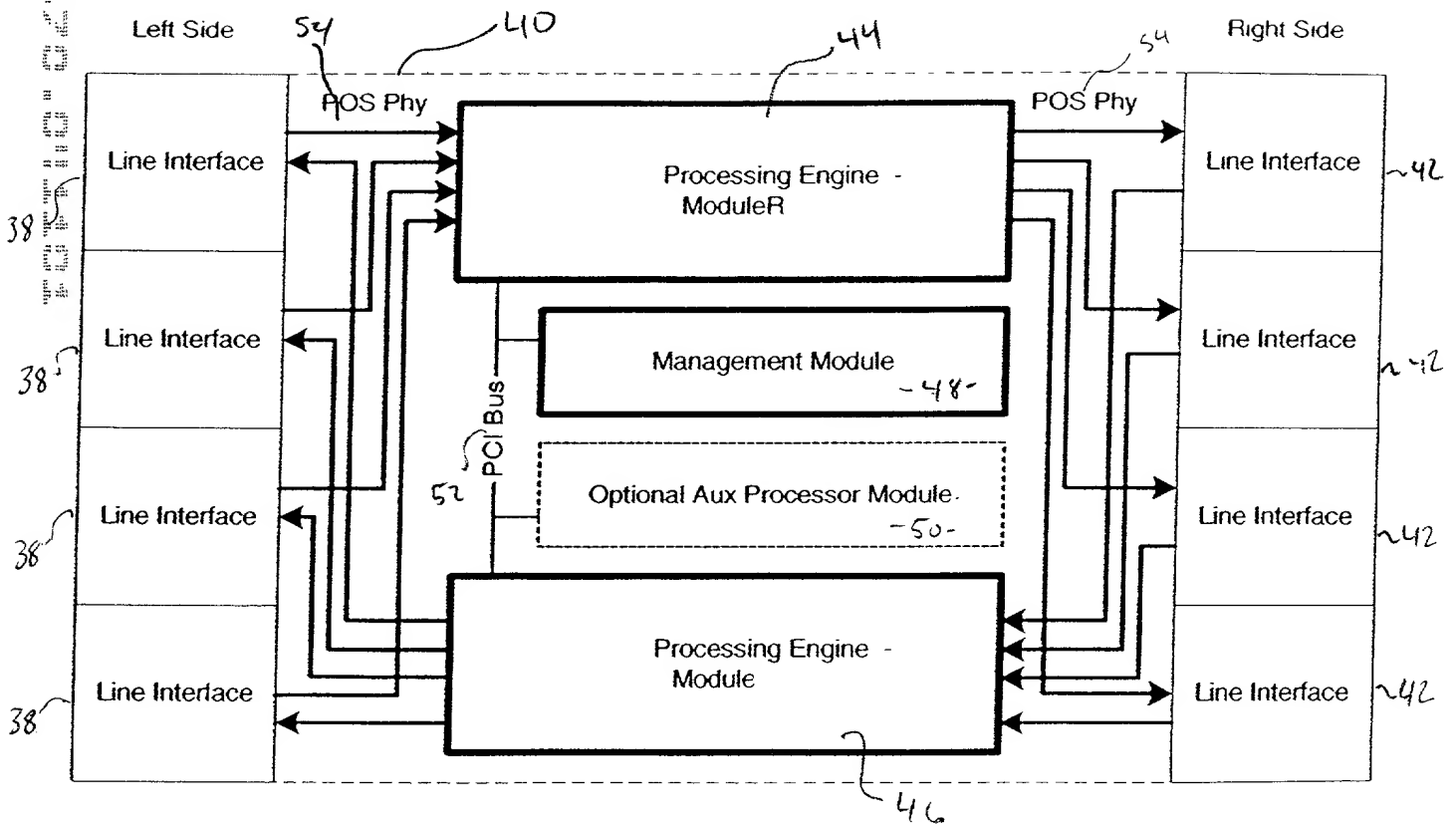


FIG. 3

FIG. 4 is a block diagram of a system architecture showing two modules, ModuleL and ModuleR, connected via a central bus system. The diagram includes various components such as uProc, Bridge, IF Control, ASI, HPP, QoS, and CP, along with their interconnections and external interfaces.

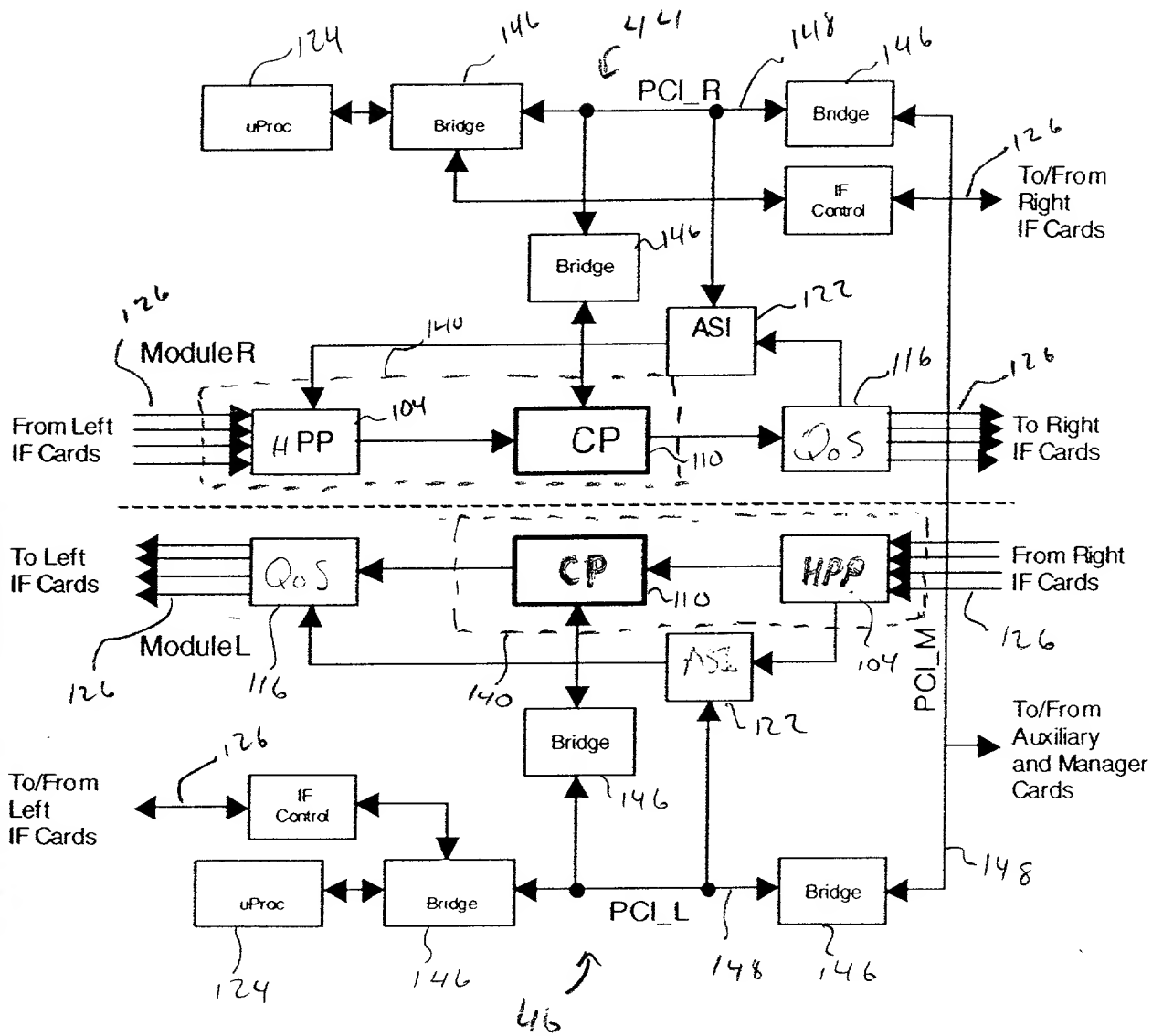


FIG. 4



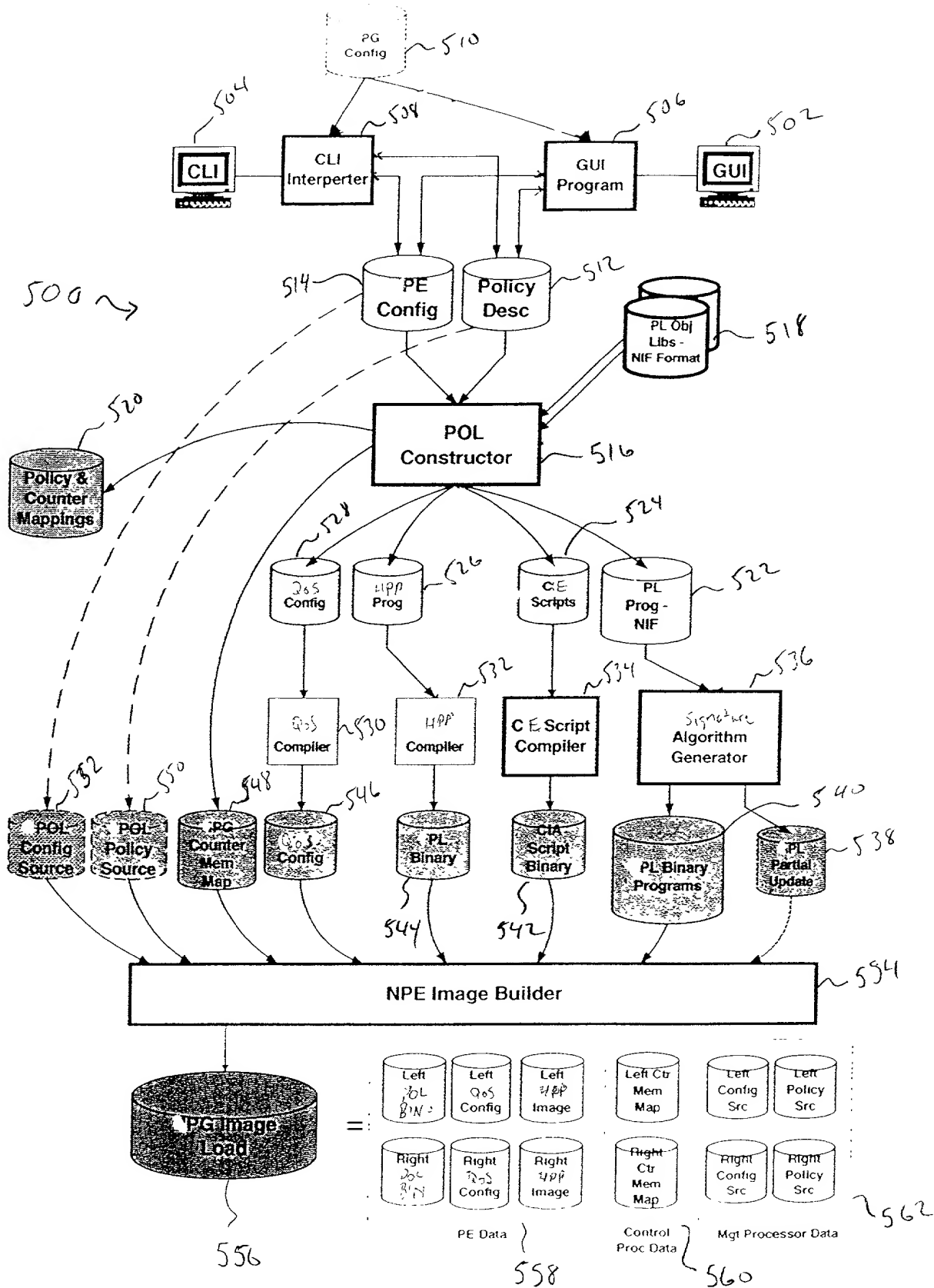


FIG 6

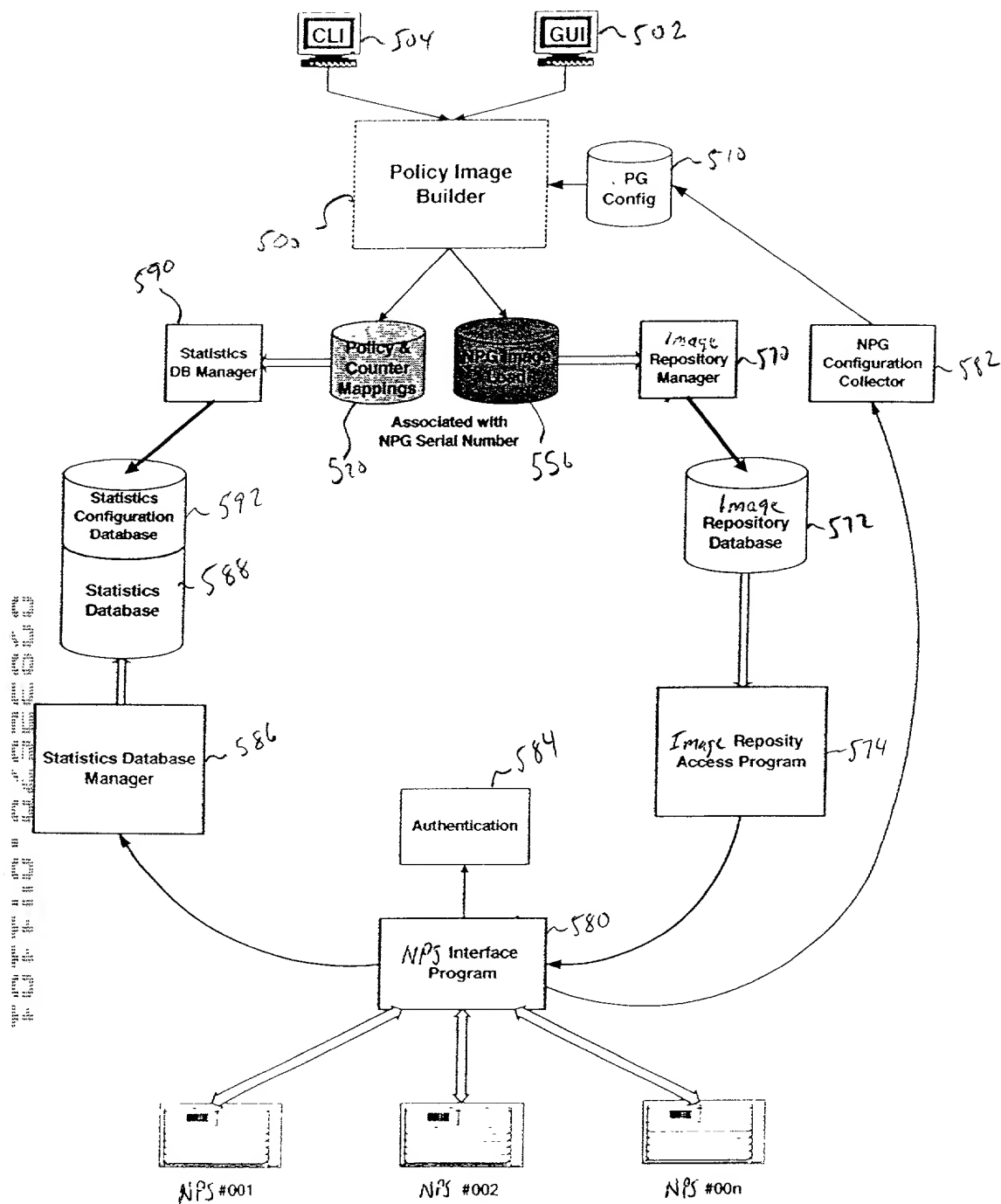


FIG. 7